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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/735,996	12/15/2003	G. Glenn Henry	CNTR.2152	2970

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EXAMINER	
FENNEMA, ROBERT E	
ART UNIT	**PAPER NUMBER**
2183	

NOTIFICATION DATE	DELIVERY MODE
09/04/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PTO@HUFFMANLAW.NET

Office Action Summary	Application No.	Applicant(s)	
	10/735,996	HENRY ET AL.	
	Examiner	Art Unit	
	Robert E. Fennema	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-5,8-11,13-15,17-25 and 27-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3-5, 8-11, 13-15, 17-25, and 27-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1, 3-5, 8-11, 13-15, 17-25, and 27-29 have been considered. Claims 1, 11, and 21 amended as per Applicant's request.

2. It is noted that the Examiner of Record has changed for this case. Future correspondence may be directed to Robert Fennema (contact information at the conclusion of this action).

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 11 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over the background of the specification (herein Henry), in view of Philip et al. (US Patent 3,130,387, herein Philip).

1. As per Claim 1, Henry teaches: A microprocessor apparatus, for precluding a pipeline stall due to microcode ROM access delay, the microprocessor apparatus comprising:

a translator, configured to generate a plurality of micro instruction queue entries, each of said plurality of micro instruction queue entries corresponding to an instruction,

and said each of said plurality of micro instruction queue entries comprising a plurality of micro instructions and a microcode entry point, wherein said translator generates said each of said plurality of micro instruction queue entries in order (Background, Paragraph 7);

a microcode ROM, configured to provide a second part of a micro instruction sequence corresponding to said microcode entry point (Paragraph 9); and

early access logic, coupled to said micro instruction queue, configured to employ a selected microcode entry point from a selected one of said plurality of micro instruction queue entries to access said microcode ROM prior to when said selected microcode entry point is provided to said register logic (Paragraph 9, it is provided during translation, thus before being provided to register logic), whereby said microcode ROM provides a first micro instruction from said second part to said register logic when said first micro instruction is required by said register logic (Paragraph 9, as the last instruction is generated from the translator, the first part of the ROM (second part) arrives at the register logic), and wherein said early access logic employs said selected microcode entry point when said selected microcode entry point is positioned within said micro instruction queue a number of entries prior to transfer to said register logic that is equal to the number of excess clock cycles exhibited by the microcode ROM access delay over that already compensated for by configuration of said translator and said micro instruction queue, but fails to teach:

a micro instruction queue, coupled to said translator, configured to receive said each of said plurality of micro instruction queue entries in said order, and configured to

provide said each of said plurality of micro instruction queue entries to register logic in said order.

While Henry teaches the translator, the ROM and logic to access the ROM, Henry does not mention the use of a micro instruction queue (essentially a buffer). However, there is a problem posed by Henry (which has caused the need for the ROM in the first place) in that there can be synchronization difficulties when dealing with hardware which does not operate at the same speed of one another. Philip however, has taught a common way to deal with this problem is to implement a buffer, which takes inputs at one rate, and outputs at another, so to overcome this problem (Column 1, Lines 28-35). Given this advantage (and need), one of ordinary skill in the art at the time the invention was made would have been motivated to make use of a buffer to take in instructions from the translator, and output them in the same order (which is what a buffer does) to the rest of the logic, to overcome any synchronization problems.

Independent Claims 11 and 21 are substantially similar to Claim 1, and are rejected for the same reasons and grounds as noted above.

3. Claims 1, 3-5, 8-11, 13-15, 17-25 and 27-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Carbine et al. (US Patent 5,222,244, herein Carbine) in view of Henry.

4. As per Claim 1, Carbine teaches: A microprocessor apparatus, for precluding a pipeline stall due to microcode ROM access delay, the microprocessor apparatus comprising:

a translator, configured to generate a plurality of micro instruction queue entries (Column 6, Line 58 – Column 7, Line 23), each of said plurality of micro instruction queue entries corresponding to an instruction, and said each comprising a plurality of micro instructions and a microcode entry point (Column 6, Lines 58-68; Column 7, Lines 1-19);

a microcode ROM, configured to provide a second part of a micro instruction sequence corresponding to said microcode entry point (Column 7, Lines 17-19; Column 8, Lines 39-46);

early access logic, coupled to said micro instruction queue, configured to employ a selected microcode entry point from a selected one of said plurality of micro instruction queue entries to access a microcode ROM prior to when said selected microcode entry point is provided to register logic, whereby said microcode ROM provides a first micro instruction to said register logic when said first micro instruction is required by said register logic (Column 8, Lines 39-46), but fails to teach:

wherein said translator generates said each of said plurality of micro instruction queue entries in order;

wherein said early access logic employs said selected microcode entry point when said selected microcode entry point is positioned within said micro instruction queue a number of entries prior to transfer to said register logic that is equal to the

number of excess clock cycles exhibited by the microcode ROM access delay over that already compensated for by configuration of said translator and said micro instruction queue.

While Carbine does teach a translator (which is not a direct translator, but a translation ROM), and early access logic which allows the translation ROM to get the inputs ahead of time, so that there will not be an interruption in the instruction flow (Column 8, Lines 39-46), Carbine does not necessarily teach that the queue entries are generated in order, and additionally, Carbine does not teach that the early access logic is used to access the ROM when the entry point is equal to the number of excess clock cycles exhibited by the ROM over that already compensated for by the translator and the micro instruction queue. However, the applicant has disclosed as prior art that the combination of a microcode ROM and a direct translator for the sequencing of macroinstructions is known in the art.

The combination of the microcode ROM and a direct translator in coordination with the microcode queue would be a viable, beneficial solution in Carbine.

An opposing possibility would be to statically populate the queue with the most commonly used instructions. One of ordinary skill in the pertinent art would have recognized that this would not be extremely useful because it would only provide the benefits of not stalling on a microcode ROM instruction in the instance of encountering a common instruction, which might not extend across different applications. In contrast, a queue that is dynamically populated by a translator when the microcode ROM instruction is first encountered will provide the benefits of the invention to all microcode

ROM instructions. Therefore, it would have been obvious to one of ordinary skill in the pertinent art at the time of the applicant's invention that providing a translator to generate the microinstruction queue entries in Carbine would provide the benefit of not stalling on any microcode ROM instruction, rather than a select few.

What cannot be inferred by this combination, however, is that said early access logic employs said microcode entry point is within a bottom micro instruction queue entry, said bottom micro instruction queue entry comprising one of said each, and wherein said bottom micro instruction queue entry will be provided to said register logic during a next clock cycle. This is because there is no evidence that Carbine's microcode translation ROM is a FIFO queue. The combination suggested could very well just put the next entry in the first available slot.

However, since it has been established that the entries would have to be provided to the register logic in the order that they were created, this would mean that each entry would need a tag associated with it, numbered to correspond to when it was entered into the queue. One of ordinary skill in the pertinent art however will realize that this creates some obstacles. Comparing tags in any unstructured (i.e. randomly ordered) storage area is time consuming. The extra field required to mark all of the entries also uses up space and wastes power. On the other hand, keeping the entries in order means only having to check one register to see where the head of the queue is – quick and easy. Therefore, one of ordinary skill in the pertinent art would be motivated to use a structured FIFO queue rather than a random queue.

As for the remaining limitation, Henry teaches that it is known in the art to use this microcode ROM to fetch microcode instructions, when the number of instructions exceeds what the ROM can generate in it's delay time, and to access it such that the instructions will be ready to issue by the time the direct translation is finished. Examiner believes that one of ordinary skill in the art would recognize that if the entry point is equal to the number of clock cycles that the ROM is delayed, then it would clearly fall into the situation described in Paragraph 9 of Henry, thus one of ordinary skill in the art at the time the invention was made would have recognized that the way to implement the invention of Henry, one would use the requirement claimed above to determine if the ROM should be accessed.

Claims 11 and 21 are substantially similar to Claim 1, and are rejected for the same reasons and grounds as discussed above.

5. As per Claim 3, Carbine teaches the microprocessor apparatus as recited in claim 1, but fails to teach: wherein said plurality of micro instruction queue entries comprises four micro instruction queue entries.

However, this limitation would have been obvious to one of ordinary skill in the art. Four entries provides a simpler design with a lower latency than designs with a greater number of entries. Further, less than four entries would not be beneficial because there would not be enough entries to make the additional logic beneficial.

In addition, it has been found that changing the size of an element does not designate a patentable difference if the invention would operate in the same manner. In re Rose, 220 F.2d 459, 463, 105 USPQ 237, 240 (CCPA 1955).

Therefore, it would have been obvious to one of ordinary skill in the pertinent art that providing four entries in Carbine would provide the benefits of a simple logic and low latency while still providing the overall benefits of the invention.

6. As per Claim 4, Carbine teaches: The microprocessor apparatus as recited in claim 1, wherein said plurality of micro instructions comprises three micro instructions (Column 7, Lines 8-11).

7. As per Claim 5, Carbine teaches:The microprocessor apparatus as recited in claim 4, wherein the microcode ROM access delay comprises four clock cycles (It is inherent that the delay is 4 cycles since the queue contains the first three instructions).

8. As per Claim 8, Carbine teaches: The microprocessor apparatus as recited in claim 1, wherein said translator is configured to provide a generated micro instruction queue entry to a top micro instruction queue entry, wherein said top micro instruction queue entry comprises one of said each micro instruction queue entry (This corresponds to the common FIFO definition of a queue, which is taught by the combination for the reasons listed above).

9. As per Claim 9, Carbine teaches: The microprocessor apparatus as recited in claim 7, wherein said translator is configured to provide a generated micro instruction queue entry to a mux, and, when said plurality of micro instruction queue entries is empty, said mux provides said generated micro instruction queue entry to said register logic during a next clock cycle (It would have been obvious to one of ordinary skill in the pertinent art that if the queue is used in a FIFO manner where an entry is dequeued each cycle, an entry enqueued to an empty queue will take 5 cycles to reach the register logic which negates the purpose of the queue. Therefore, a bypass from the translator to the register logic would have been an obvious variation to one of ordinary skill in the pertinent art.).

10. As per Claim 10, Carbine teaches: The microprocessor apparatus as recited in claim 9, wherein said early access logic employs a bypass microcode entry point corresponding to said generated micro instruction queue entry (It is obvious that an entry point to the ROM will still need to be generated since the ROM will still need to be accessed after the first three instructions.).

11. Claims 13-15,17-25 and 27-29 contain similar limitations to those of claims 1, 3-5, 8-11 and are therefore rejected for the same reasons.

Response to Arguments

12. For both grounds of rejection, the Applicant has essentially argued the same thing, that the combination of references in both cases does not teach the amended claim language regarding the early access logic, namely, the limitation which indicates when to use the entry point and the microcode ROM (when it is positioned within said micro instruction queue a number of entries prior to transfer to said register logic that is equal to the number of excess clock cycles exhibited by the microcode ROM access delay over that already compensated for by configuration of said translator and said micro instruction queue. While the Examiner appreciates the Applicant's attempt to overcome the art by going into more detail of the early access logic, Examiner is not convinced that the amendment overcomes the background of the invention. The background discloses that the microcode ROM is used when there are a corresponding number of micro instructions to be executed, which are in greater number than what could be generated during the access delay time (Paragraph 9), and in this situation, both methods are used, such that the ROM access time is absorbed by the translation time.

Now, while that does not specifically use the same language as is in the claim, Examiner believes that it would have been obvious to come to that limitation from the specification. The specification teaches under what situation to use the ROM and translator, and also teaches that when it is used, that the ROM will output the second part when it is needed. Based on these statements, one of ordinary skill in the art would

have recognized that in order to use the invention as described in Paragraph 9, that the entry would have to be positioned in the manner described in the claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert E. Fennema whose telephone number is (571) 272-2748. The examiner can normally be reached on Monday-Friday, 8:45-6:15.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Robert E Fennema
Examiner
Art Unit 2183

RF